Initial SEE Tests of SanDisk Flash Memory

Introduction

Initial SEE tests of SanDisk nonvolatile memory cards were done on September 20, 1997 at Brookhaven National Laboratory. Two versions of the memory devices were available, with feature sizes of 0.5 and 0.4 µm. The SanDisk memory cards contain a proprietary controller chip that emulates a disk drive, and provides all control signals for the flash memories, including the high voltage required to erase and write these devices. The controller chip is fabricated by a different foundry than the flash memory devices. Because the control chip and memory elements are physically separated, it is easier to diagnose SEE failure modes in the control and memory elements for the SanDisk devices compared to other flash memory technologies.

SanDisk agreed to supply most of the hardware for the tests, as well as an engineer to assist in diagnosing test results. They supplied adapters for the memory devices. They also checked out their hardware and software to make sure that it would function with longer cable lengths (approximately six feet) that are required at the accelerator. However, as discussed below, the hardware did not function properly at the test site, which limited the test results. Nevertheless, the test results were able to identify functional errors in the controller. It also appears that the control and memory devices are not susceptible to latchup.

Initial Testing with JPL Interface

Before the SanDisk engineer arrived, JPL personnel did some initial tests on the 0.5µm devices using a simplified interface that involved relatively slow read/write operations, essentially treating the memory system as a floppy disk. There was a problem with the pins on the first adapter (poor contact with a damaged pin) that caused failure of the first two 0.5µm devices during checkout and setup. After the adapter problem was identified, the second adapter was used for tests of the third 0.5 µm device.

Separate runs with bromine ions (LET = 35 MeV-cm^2/mg) were used to test the controller and memory chips individually, changing the physical location of the board to determine which device was exposed to the ion beam. During the first run, only the memory chip was irradiated with a total fluence of 5×10^5 ions/cm^2. The memory was operated statically, with no read or write operations during irradiation. No functional errors were observed and the memory system continued to function properly during read/verify operational tests after the irradiation.

The second run (also to a fluence of 5×10^5 ions/cm^2) exposed only the controller chip to the beam, applying bias, again with no read or write operations during irradiation. At the end of the run, the memory could no longer be accessed properly. The diagnostics showed "General Drive Failure," however, proper operation could be restored by cycling power. No significant changes occurred in the power supply current, suggesting that this effect was caused by a functional change in the controller, not latchup.

The third run duplicated the conditions of the first run, exposing only the memory device, but using twice the fluence (1×10^6 ions/cm^2). Again, no malfunctions occurred when the memory was functionally tested after the completion of the test. Although these test results are somewhat limited, the fact that no malfunctions occurred when testing the memory chip indicates that SEE effects are insignificant for applications that do not involve active read or write operations. The upsets that were observed in the controller suggest that the control chip is the most susceptible part of the memory system. A crude estimate of the upset cross section is $> 10^{-6}$ cm^2 at a LET of 35 MeV-cm^2/mg, but latchup did not occur with this ion (within the limitations of the cross section estimate corresponding to 10^6 ions/cm^2).

Tests with SanDisk Hardware

When the SanDisk engineer arrived, an additional test run was made on the remaining 0.5µm device card memory chip, using the SanDisk-developed hardware and software. This involved data transfer at much higher speed than the simplified interface used by JPL in the first three test sequences. Although the memory card worked initially, it failed after irradiation with 10^6 ions/cm^2, but worked satisfactorily when tested with the simplified JPL interface.

We attempted to test the 0.4 µm device cards using the SanDisk hardware and software. However, the 0.4 µm devices would not function properly, and the reason for this difficulty could not be determined at the test site. Consequently, no test results are available for the 0.4 µm memory.

Conclusions

Although not all the test goals were met, initial test results indicate that the control chip is the most susceptible part of the SanDisk memory system. This chip is used in all of the SanDisk memory cards, and it is likely that its SEE sensitivity will be the limiting factor in applications in space.

The results of the tests with bromine ions are summarized in Table 1, below. These tests are limited in scope, using the memory in a static mode. However, they are consistent with more thorough evaluations of other flash memory technologies (without external control chips) that have shown that SEE in the control circuitry, not the memory elements, is the dominant problem for flash memories[1]. Those results showed that the cross section for control errors is low, ~ 10^{-6} to 10^{-5} cm^2, consistent with the cross section expected for errors in individual control bits or registers.

Additional work is required to characterize the SanDisk devices for applications in space. It appears likely that the control chip is the weak link. A second series of tests using ions with lower LETs, and lower total fluences is recommended to establish the cross section. It would also be helpful to do initial evaluations of the SanDisk hardware and software with the JPL californium source before additional tests are done to insure compatibility with the long leads, connectors, and timing limitations in the radiation test chamber.

[1] H. R. Schwartz, D. K. Nichols, and A. H. Johnston, "Single-Event Upset in Flash Memories," presented at the 1997 Nuclear and Space Radiation Effects Conference, Snowmass Colorado, July 25, 1997; accepted for publication in the IEEE Transactions on Nuclear Science, December, 1997.